RAM and ROM Chips

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RAM Chip

- RAM is the main memory.
- It has bidirectional data bus that allows the transfer of data either from memory to CPU during a read operation or from CPU to memory during a write operation.
- The capacity of the memory is 128 words of eight bits (one byte) per word.
- This requires a 7-bit address and an 8-bit bidirectional data bus.
- The read and write inputs specify the memory operation and the two chip select (CS) control inputs are for enabling the chip only when it is selected by the processor.

<table>
<thead>
<tr>
<th>CS&lt;sub&gt;1&lt;/sub&gt;</th>
<th>CS&lt;sub&gt;2&lt;/sub&gt;</th>
<th>RD</th>
<th>WR</th>
<th>Memory Operation</th>
<th>State of Data Bus</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>X</td>
<td>X</td>
<td>No Operation</td>
<td>High Impedance</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>X</td>
<td>X</td>
<td>No Operation</td>
<td>High Impedance</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>No Operation</td>
<td>High Impedance</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Write Operation</td>
<td>Input Data to RAM</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>X</td>
<td>X</td>
<td>Read Operation</td>
<td>Output Data from RAM</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>X</td>
<td>X</td>
<td>No Operation</td>
<td>High Impedance</td>
</tr>
</tbody>
</table>

ROM Chip

- ROM can only read, the data bus can only be in an output mode.
- For the same size chip, it is possible to have more bits of ROM than of RAM, because the internal binary cells in ROM occupy less space than in RAM.
- For this reason, the diagram specifies a 512 byte ROM, while the RAM has only 128 bytes.
- The nine address lines in the ROM chip specify any one of the 512 bytes stored in it.

Memory Address Map

- A memory address map is a pictorial representation of assigned address space for each chip in the system.
- Let us assume that a computer system needs 512 bytes of RAM and 512 bytes of ROM.
- The RAM chips have 128 bytes and need seven address lines. The ROM chip has 512 bytes and needs 9 address lines.
- The X’s are always assigned to the low order bus lines: lines 1 through 7 for the RAM and lines 1 through 9 for the ROM. It is now necessary to distinguish between 4 RAM chips by assigning each to a different address.
MEMORY CONNECTION TO CPU

- The configuration gives a memory capacity of 512 bytes of RAM and 512 bytes of ROM.

- The particular RAM chip selected is determined from lines 8 and 9 in the address bus. This is done through a 2 x 4 decoder whose outputs go to the CS inputs in each RAM chip.

- The selection between RAM and ROM is achieved through bus line 10.

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Table 5.5: Memory Address Map for Microcomputer