RAM and ROM Chips

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RAM Chip

- RAM is the main memory.
- It has bidirectional data bus that allows the transfer of data either from memory to CPU during a read operation or from CPU to memory during a write operation.
- The capacity of the memory is 128 words of eight bits (one byte) per word.
- This requires a 7-bit address and an 8-bit bidirectional data bus.
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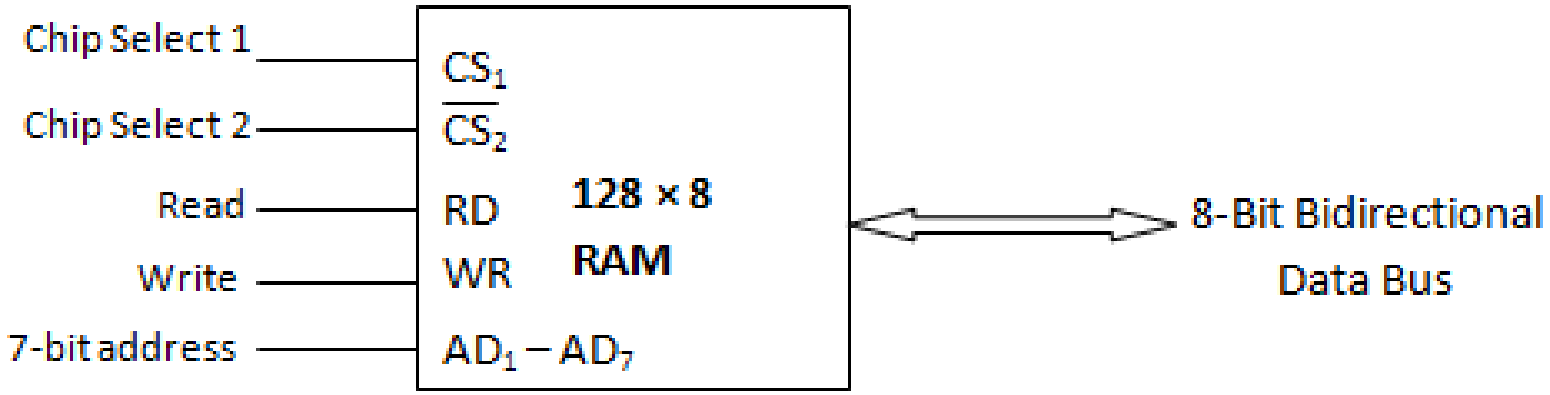
- The *read* and *write* inputs specify the memory operation and the two *chip select* (CS) control inputs are for enabling the chip only when it is selected by the processor.

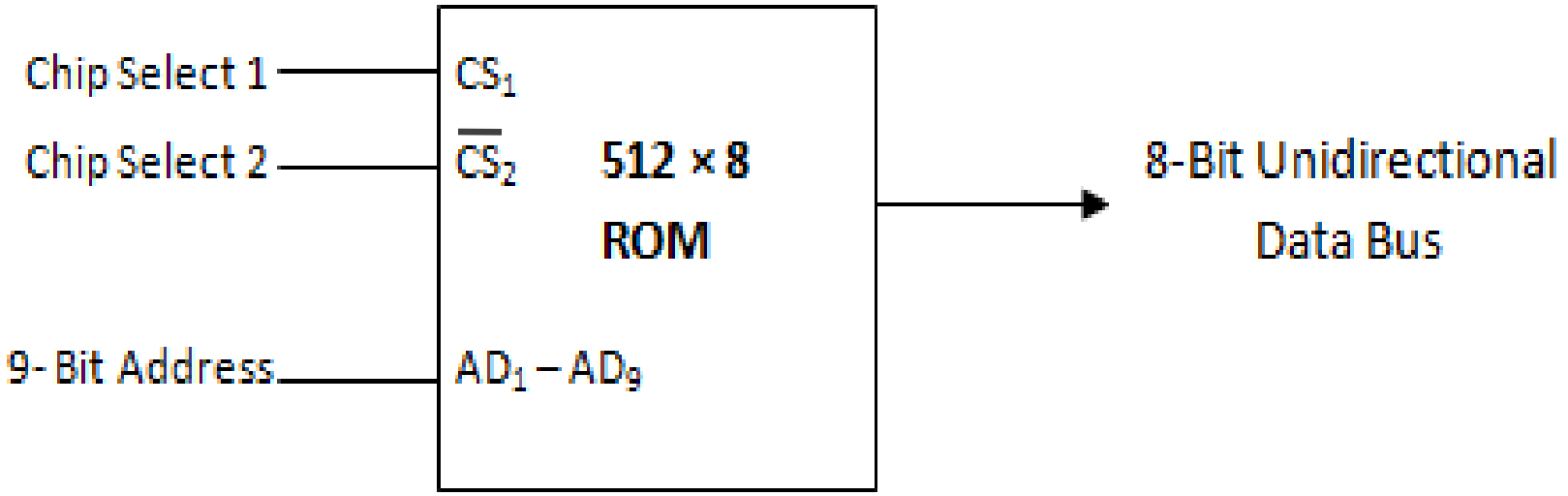


CS_1	CS_2	RD	WR	Memory Operation	State of Data Bus
0	0	X	X	No Operation	High Impedance
0	1	X	X	No Operation	High Impedance
1	0	0	0	No Operation	High Impedance
1	0	0	1	Write Operation	Input Data to RAM
1	0	1	X	Read Operation	Output Data from RAM
1	1	X	X	No Operation	High Impedance

ROM Chip

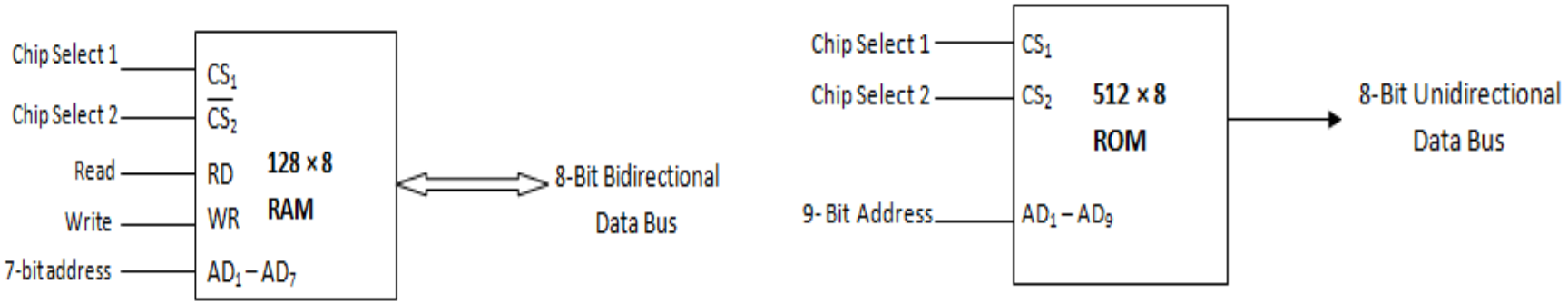
- ROM can only read, the data bus can only be in an output mode.
- For the same size chip, it is possible to have more bits of ROM than of RAM, because the internal binary cells in ROM occupy less space than in RAM.
- For this reason, the diagram specifies a 512 byte ROM, while the RAM has only 128 bytes.
- The nine address lines in the ROM chip specify any one of the 512 bytes stored in it.

ROM Chip


Chip Select 1
Chip Select 2
9- Bit Address
CS_1
$\overline{CS}_2$
$AD_1 - AD_9$
512 × 8
ROM
8-Bit Unidirectional
Data Bus

Memory Address Map

- *A memory address map*, is a pictorial representation of assigned address space for each chip in the system.
- Let us assume that a computer system needs 512 bytes of RAM and 512 bytes of ROM
- The RAM chips have 128 bytes and need seven address lines. The ROM chip has 512 bytes and needs 9 address lines.
- The X's are always assigned to the low order bus lines: lines 1 through 7 for the RAM and lines 1 through 9 for the ROM. It is now necessary to distinguish between 4 RAM chips by assigning to each a different address.

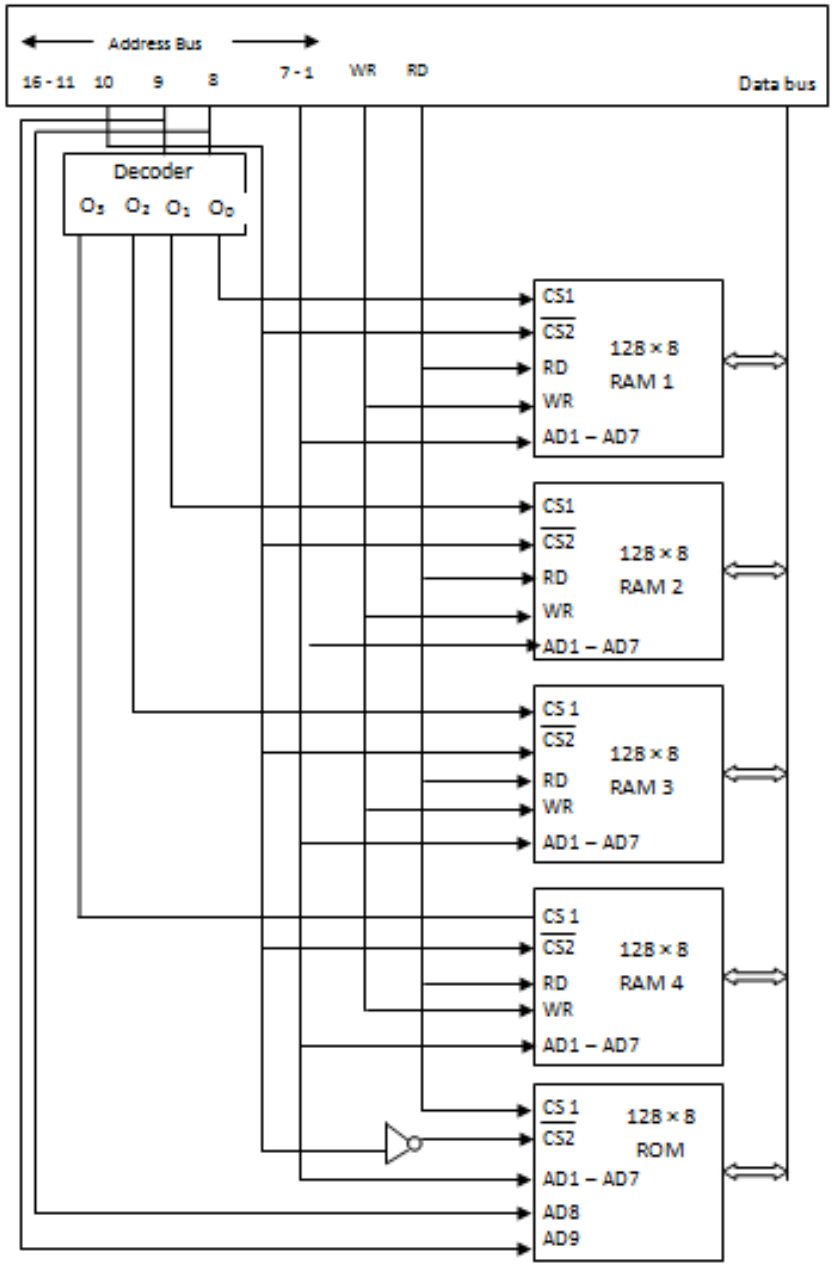


Device Select	Hexadecimal Address	10	9	8	7	6	5	4	3	2	1
RAM 1	0000 – 007F	0	0	0	X	X	X	X	X	X	X
RAM 2	0080 – 00FF	0	0	1	X	X	X	X	X	X	X
RAM 3	0100 – 017F	0	1	0	X	X	X	X	X	X	X
RAM 4	0180 – 01FF	0	1	1	X	X	X	X	X	X	X
ROM	0200 – 03FF	1	X	X	X	X	X	X	X	X	X

Table 8.5: Memory Address Map for Microcomputer

MEMORY CONNECTION TO CPU

- The configuration gives a memory capacity of 512 bytes of RAM and 512 bytes of ROM.
- The particular RAM chip selected is determined from lines 8 and 9 in the address bus. This is done through a 2 x 4 decoder whose outputs goes to the CS_1 inputs in each RAM chip.
- The selection between RAM and ROM is achieved through bus line 10.


Address Bus
16 - 11
10
9
8
7 - 1
WR
RD
Data bus
Decoder
O3 O2 O1 O0
CS1
CS2
RD
WR
AD1 – AD7
128 × 8
RAM 1
CS1
CS2
RD
WR
AD1 – AD7
128 × 8
RAM 2
CS 1
CS2
RD
WR
AD1 – AD7
128 × 8
RAM 3
CS 1
CS2
RD
WR
AD1 – AD7
128 × 8
RAM 4
CS 1
CS2
AD1 – AD7
AD8
AD9
128 × 8
ROM

THANKS A LOT