PUNJAB COLLEGE OF TECHNICAL EDUCATION

COURSE – PLAN (Jan 10 – May 10)

SUBJECT:	Digital Circuits & Logic Design
CODE:	BC – 205 (N2)
CLASS:	BCA – 2nd Sem
SECTION:	C
TEACHERS:	Mr. Gursharan Singh (GS)

Course Description:

The course teaches digital design fundamentals for combination logic circuits along with an introduction to sequential logic circuits. The aim of this course is to provide an understanding of the fundamentals of digital logic design to the students. The course encompasses the fundamental concepts such as number systems, codes, and logic gates. It develops into the design of combinational and sequential logic circuits.

More specifically, we will cover the following topics:

- Introduction to Digital Circuits
- Boolean Algebra
- Combinational Logical Circuits
- Sequential Logic Circuits
- Counters
- Registers
- Detection and Correction Codes

Course Goals:

The objective of this course is to:

- Understand the fundamentals of digital logic, such as number systems and codes.
- Understand the basic logic gates.
- Analyze digital logic circuits.
- Design and build combinational logic circuits.
- Design and build sequential logic circuits.
- Understand and design some practical digital circuits.

Grading:

MSE:	15 marks
1st One Hourly Test:	5 marks
2nd One Hourly Test:	5 marks
Presentation:	5 marks
Class Tests:	5 marks
Assignments:	5 marks
Total:	**40 marks**

Rules for Assignments:

Purpose:

The assignments will primarily be practice problems for the exams. Thus, you should not collaborate on it with others by splitting the work and sharing answers. You will gain the most benefit from doing it by yourself. You can, of course, ask me for help. If someone in the class asks you for help on assignments, handle the situation as if you are a course instructor. Don't just give them an answer, but make sure they know how to find the answer on their own. ***If I feel that people have submitted answers that are merely copies of each other, I will grade the one solution and divide the credit for it equally among the copies.***

Due Date:

As indicated in the course break-up below.

Late Policy:

You must do your work on time because we'll be correcting/discussing it in class. ***No assignment will be accepted after the due date.*** If you know that you have a specific time conflict, make arrangements with me in advance for a separate assignment for late submission.

Format:

All assignments should be done according to the following format:

- Assignment must have a cover page including *title of assignment, subject, date of submission, students name, class, roll no.* and *submitted to*.
- For a sample of cover page, visit my website http://www.eazynotes.com.
- Use loose sheets with one side plain and other side lined.
- Write questions/headings with black pen and other text with blue pen.

- Draw diagrams (if necessary), neat and clean with pencil on plain side of paper.
- Pages should be numbered.
- Mention ***Contents*** at the beginning and ***References*** at the end of each assignment.

Tests:

Tests can be oral/written/open book. Open book test is so that you can look up formulas or data from the text or lecture notes. You need to be sufficiently familiar with the material in the book to know where to look up the information that you need. The purpose of the exams is for you to demonstrate that you have attained an operational level of understanding of the material.

The tests will be conducted on the dates mentioned in the course break-up. No extra test will be conducted for the absentees. If you have any time conflict for the test, contact me in advance so that we can make sufficient arrangements. Keep in mind that there will be no improvement test at the end of the semester. Therefore, its your responsibility to give test on time.

Presentation:

One presentation will be held for this subject. You will be informed well in advance. The rules for presentation are as follows:

- Group will be of 3-4 students.
- Students can make groups of their choice.
- Students should be in strict formals for the presentation.
- Three attendances will be taken during presentation. One at sharp 9:00 am, second after lunch break, and third at the end of the presentation.
- ***Present*** will be counted only for those students who'll be present in all the three attendances.
- Marks will be given only to the present students.
- If the student is absent, I will deduct (– 10) marks for it.
- Marks will be deducted for each misbehavior/indiscipline during the presentation.
- Topics will be given at first-cum-first-get basis. No topic will be repeated.

- Marks for the presentation are distributed as follows:

Dress:	10 marks
Report:	10 marks
Synopsis:	5 marks
Content:	5 marks
Slides:	5 marks
Confidence:	5 marks
Query Handling:	10 marks
Total:	**50 marks**
Absent:	– 10 marks
Indiscipline:	– 1 marks (for each misbehavior)

Class Participation:

A large component of your learning takes place in class. The actual concepts of DLCD are fairly simple, although their implementation is often complicated by real-world constraints. Thus, I tend to give lectures to explain these concepts, and pose questions for discussion that are meant to draw out these implications. I will guide discussion, and add information here and there as necessary to carry the discussion forward or to lead it into a digression that adds depth in a different direction.

I will frequently have in-class exercises that you will do as individual/groups. Thus, it is very important that you attend class regularly. I will keep attendance throughout the semester. Please let me know in advance of any scheduled absences.

It is very important that we focus our attention during the limited time we have together. Each of us comes to the classroom distracted by thoughts from outside. Thus, each day we will take about two minutes at the beginning with a brief mind-clearing exercise, followed by a focusing exercise. During the mind-clearing exercise we will sit in silence and concentrate on our breathing. Because it is important that we not be distracted while doing these exercises, I will close the door promptly at the starting time for class. If you arrive late and the door is already closed, please wait outside until I reopen it and invite you in.

Classroom Policies:

Following are the classroom policies and they are meant to be strictly followed:

- Be punctual for the class, try to minimize your disturbance if you are late. I may reject students who come after 15 minutes from the scheduled time.
- Student coming late will be considered as ***late arrival*** and I will record late arrivals on the day's attendance.
- Three late arrivals equals to one absent.
- Mobile phones are not allowed in the classroom. If any student found using the mobile phone, he/she has to pay Rs. 200 as fine in the account office.
- During lecture delivery, if you have any kind of query, just raise your hand. Queries are important for the understanding of the concepts. So, do ask queries but make sure they are relevant to the subject.
- Be disciplined in the classroom and don't make any noise while we are studying.

SYLLABUS

DIGITAL CIRCUITS & LOGIC DESIGN

BC – 205 (N2) **Internal Assessment: 40**

Max. Marks: 100 **External Assessment: 60**

Instructions for paper setter:

The question paper will consist of two sections A and B. Sections B will have Six questions and will carry 10 marks each. Section A will have 10 short answer type questions, which will cover the entire syllabus uniformly and will carry 20 marks in all.

Instructions for Candidates:

Candidates are required to attempt four questions from section B and the entire section A. Use of nonprogrammable scientific calculator is allowed.

Introduction: Overview of number system and codes. Elements and functions of digital Logic gates, Gate propagation delay time, logic gates applications.

Boolean Algebra: Boolean operations, SOP and POS forms, and simplification using karnaugh maps, Realization of expressions using goals.

Combinational Logical Circuits: Design of Binary Adder-Serial, Parallel, Carry look ahead type. Full Subtractor, code converters, MUX and DEMUX, encoders and encoders.

Sequential Logic Circuits: Flip flop: R-S, J-K, Master slave J-K, D and T flip-flops using nand gates.

Counters: Design of asynchronous and synchronous, updown and programmable counters.

Registers: Shift registers, various types and their applications.

Detection and correction codes, detecting and correcting an error.

COURSE BREAK-UP

Subject:	Digital Circuits & Logic Design	**Code:**	BC – 205 (N2)
Class:	BCA	**Semester:**	II
No. of Lect.:	48	**No. of Assignments:**	3
Teachers:	Mr. Gursharan Singh (GS)	**No. of Tests:**	3

Proposed Week	Lect. No.	Lect. Content	Assignments	Tests	Actual Date of Delivery
1	1.	Introduction to Course Plan			
	2.	Introduction to DCLD			
	3.	Number System & Conversion of one number system to another			
	4.				
2	5.	Arithmetic operation without changing the base			
	6.	1's compliment and 2's compliment			
	7.	Codes	Assign-1		
	8.	Error Detection and Correction Codes			
3	9.				
	10.	Logic Gates & Switching circuits			
	11.	NAND and NOR as universal Gates			
	12.	Logic Gates Applications			
4	13.			Test-1	
	14.	Introduction to Boolean Algebra			
	15.	SOP and POS forms of Boolean equations			
	16.	Realization of Boolean expression using Gates			
5	17.	K-Maps & Simplification of Boolean Expression using K-Maps			
	18.				
	19.	Combinational Logic Circuits			
	20.	Half Adder & Half Subtractor			
6	21.	Full Adder & Full Subtractor			
	22.	Serial Binary Adder Parallel Binary Adder			

		Carry Look Ahead Adder			
	23.	Binary Adder/Subtractor	Assign-2		
	24.	Code Converters			
7	25.				
	26.	MUX & DEMUX			
	27.	Implementation of Boolean equations using MUX and DEMUX			
	28.	Encoders & Decoders			
8	29.			Test-2	
	30.	Sequential Circuits Flip Flops			
	31.	R-S Flip-Flop using NAND Gates			
	32.	J-K Flip-Flop using NAND Gates			
9	33.	Race Around Condition Removing Race Around Condition			
	34.	D Flip-Flop using NAND Gates T Flip-Flop using NAND Gates			
	35.	Master-Slave J-K Flip-Flop			
	36.	Edge Triggered Flip-Flops and Applications of Flip-Flops	Assign-3		
10	37.	Counters			
	38.	Design of Asynchronous or Ripple Counters			
	39.	Design of Synchronous Counters			
	40.	Up-Down Counters MOD-n Counters			
11	41.	Programmable Counters Ring Counters Twisted Ring Counters			
	42.			Test-3	
	43.	Registers			
	44.	Types of Shift Registers			
12	45.	SISO Shift Register PISO Shift Register			
	46.	SIPO Shift Register PIPO Shift Register			
	47.	Applications of Shift Registers			
	48.	Discussion of Previous Question Papers			

Textbooks and Resources:

- Digital Circuits of Logic Design
  - Author: D. Morris Mano
  - Publisher: Prentice Hall of India
- Digital and Electronic Circuits
  - Author: T. C. Bartee
  - Publisher: Tata – McGraw Hill
- Digital Computer Electronics
  - Author: Malvino
- Digital Fundamentals
  - Author: Floyd
- Modern Digital Electronics
  - Author: R. P. Jain
- Digital Integrated Electronics
  - Author: Tauls and Schillings
- Other handouts will be provided throughout the semester

ASSIGNMENT – 1

1. **Short answer type question:**
   - **a.** What is the largest decimal number that can be represented by 16-bit binary word?
   - **b.** What are the applications of binary number system?
   - **c.** Perform the following conversions:
     - **i.** 40 from decimal to octal number
     - **ii.** Convert DF from hex to decimal number
     - **iii.** $(11011.11)_2$ to decimal number
     - **iv.** $(A4F)_{16}$ to Octal number
   - **d.** Subtract $(101)_2$ from $(1011)_2$ using 2's complement.
   - **e.** Subtract $(1101)_2$ from $(1111)_2$ using 1's complement.

ASSIGNMENT – II

1. **Short answer type questions:**
   - **a.** What are universal gates?
   - **b.** Simplify $\overline{(a + b)} + \overline{(a + \bar{b})}$
   - **c.** Prove using truth table $A + \bar{A}B = A + B$?
   - **d.** Define the term Propagation Delay.
   - **e.** How can you use NAND gate as inverter?
2. **Long answer type questions:**
   - **a.** Minimize the following Using K-Map and Realize it with NAND Gates:

     $F(A, B, C, D) = \Sigma m(2, 3, 4, 5, 13, 15) + \Sigma d(8, 9, 10, 11)$
   - **b.**
     - **i.** Convert the given expression in canonical SOP form Y: AC + AB + BC.
     - **ii.** Simplify the function using Karnaugh map and implement using minimum number of logic gates. $F = \Sigma m(0, 2, 4, 7, 8, 13, 14)$

ASSIGNMENT – III

1. **Short answer type questions:**
   - a. What is Priority Encoder?
   - **b.** What is the difference between Combinational and Sequential Circuits?

c. What is the difference between Latch and a Flip-Flop?

d. What is a D-Flip Flop?

e. What do you mean by Race Around Condition?

2. Long answer type questions:

a. What is a Multiplexer? Construct a 64-to-1 multiplexer using 4 x 1 MUX.

b. Discuss the Master Slave J-K Flip Flop with the help of suitable block diagram.

LIST OF PRACTICALS

1. Verify Output of AND Gate Using IC 7408
2. Verify Output of OR Gate Using IC 7432
3. Verify Output of NOT Gate Using IC 7404
4. Verify Output of NAND Gate Using IC 7408 & IC 7404
5. Verify Output of NOR Gate Using IC 7432 & IC 7404
6. Verify Output of NAND Gate Using IC 7400
7. Verify Output of NOT Gate Using IC 7400
8. Verify Output of AND Gate Using IC 7400
9. Verify Output of NOR Gate Using IC 7402
10. Verify Output of NOT Gate Using IC 7402
11. Verify Output of OR Gate Using IC 7402
12. Verify Output of OR Gate Using IC 7400
13. Verify Output of AND Gate Using IC 7402
14. Verify Output of XOR Gate Using IC 7486
15. Verify Truth-Table of HALF ADDER
16. Verify Truth-Table of FULL ADDER
17. Verify Truth-Table of HALF SUBTRACTOR
18. Verify Truth-Table of FULL SUBTRACTOR
19. Implement 2 x 1 MUX using Basic Gates
20. Implement 1 x 2 DEMUX using Basic Gates

PRESENTATION TOPICS

1. Basic Principle of a CD Player
2. Bread-board Sockets
3. Serial vs. Parallel transfer of Binary data
4. Caller ID
5. Integrated Circuits
6. MODEM
7. Working of CRT
8. Working of LCD
9. Semi-Conductors
10. Transistors
11. Boolean Algebra
12. Basic Logic Gates
13. Universal Logic Gates
14. Canonical SOP and POS Forms
15. Half Adder / Full Adder
16. Half Subtractor / Full Subtractor
17. Parallel Binary Adder
18. 2’s Complement Adder Subtractor