PIN DIAGRAM OF 8086

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Intel 8086



Intel 8086 was launched in 1978.

- It was the first 16-bit microprocessor.
- This microprocessor had major improvement over the execution speed of 8085.
 - It is available as 40-pin Dual-Inline-Package (DIP).

Intel 8086



It is available in three versions:

- 8086 <mark>(5 MHz)</mark>
- 8086-2 (8 MHz)
- 8086-1 (10 MHz)
- It consists of 29,000 transistors.

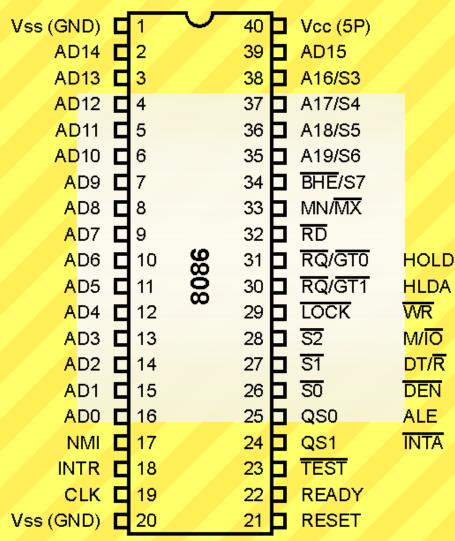
Intel 8086



It has a 16 line data bus.

- And 20 line address bus.
- It could address up to 1 MB of memory.
- It has more than 20,000 instructions.
 - It supports multiplication and division.

Pin Diagram of Intel 8086



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AD₀ – AD₁₅ Pin 16-2, 39 (Bi-directional)

- These lines are multiplexed bidirectional address/data bus.
- During T₁, they carry lower order 16-bit address.
- In the remaining clock cycles, they carry 16-bit data.
- AD₀-AD₇ carry lower order byte of data.
- AD₈-AD₁₅ carry higher order byte of data.

Vs	s (GND)		1	$\overline{}$	40	þ	Vcc (5P)	
	AD14		2		39	þ	AD15	
	AD13		3		38	Þ	A16/S3	
	AD12	С	4		37	þ	A17/S4	
	AD11	C	5		36	þ	A18/S5	
	AD10		6		35	þ	A19/S6	
	AD9		7		34	þ	BHE/S7	
	AD8	٢	8		33	þ	MN/MX	
	AD7		9		32	þ	RD	
_	AD6	С	10	86	31	þ	RQ/GT0	HOLD
	AD5		11	8086	30	þ	RQ/GT1	HLDA
- 1	AD4		12		29	þ	LOCK	WR
	AD3		13		28	þ	<u>52</u>	M/ĪŌ
	AD2		14		27	þ	<u>S1</u>	DT/R
	AD1		15		26	þ	SO	DEN
	AD0		16		25	þ	QS0	ALE
	NMI	C	17		24	þ	QS1	INTA
	INTR	Γ	18		23	þ	TEST	
	CLK		19		22	þ	READY	
Vs	s (GND)		20		21	þ	RESET	

A₁₉/S₆, A₁₈/S₅, A₁₇/S₄, A₁₆/S₃ Pin 35-38 (Unidirectional)

- These lines are multiplexed unidirectional address and status bus.
- During T₁, they carry higher order 4-bit address.
- In the remaining clock cycles, they carry status signals.

	× .							
SND)	۵	1	V	40		Vcc (5P))	
D14	۵	2		39		AD15		
D13	۵	3		38		A16/S3		
D12		4		37		A17/S4		
\D11	۵	5		36		A18/S5		
D10	۵	6		35		A19/S6		
AD9	۵	7		34	ם	BHE/S7		
AD8	۵	8		33		MN/MX		
AD7	۵	9		32	þ	RD		
AD6	۵	10	86	31		RQ/GT0	j	HOLE
AD5	۵	11	ö	30		RQ/GT1		HLDA
AD4	۵	12		29		LOCK		WR
AD3		13		28		<u>52</u>		M/ĪŌ
AD2	۵	14		27		<u>S1</u>		DT/R
AD1	۵	15		26		SO		DEN
AD0		16		25		QS0		ALE
NMI	۵	17		24		QS1		INTA
NTR	۵	18		23		TEST		
CLK	С	19		22		READY		
SND)		20		21		RESET		
	AD14 AD12 AD12 AD11 AD10 AD9 AD8 AD7 AD8 AD1 AD2 AD1 AD2 <	AD14 I AD13 I AD12 I AD14 I AD10 I AD10 I AD14 I AD3 I AD4 I A	AD14 I 2 AD13 I 3 AD12 I 4 AD11 I 5 AD10 I 6 AD19 I 7 AD3 I 3 AD4 I 10 AD5 I 11 AD4 I 12 AD3 I 13 AD2 I 14 AD1 I 15 AD0 I 16 NMI I 17 NTR I 19	AD14 I 2 AD13 I 3 AD12 I 4 AD11 I 5 AD10 I 6 AD9 I 7 AD8 I 8 AD7 I 9 AD6 I 10 80 AD5 I 11 80 AD4 I 12 80 AD3 I 13 400 AD1 I 15 400 16 NMI I 17 18 18 CLK I 19 19 19	AD14 I 2 39 AD13 I 3 38 AD12 I 4 37 AD11 I 5 36 AD11 I 6 35 AD9 I 7 34 AD8 I 8 33 AD7 I 9 32 AD6 I 10 99 32 AD5 I 11 30 30 AD4 I 12 29 30 AD3 I 13 28 30 AD1 I 15 26 35 AD0 I 16 25 35 NMI I 18 23 33 CLK I 19 22 35	AD14 I 2 39 I AD13 I 3 38 I AD12 I 4 37 I AD12 I 4 37 I AD11 I 5 36 I AD11 I 5 36 I AD11 I 6 35 I AD10 I 7 34 I AD3 I 9 32 I AD5 I 10 90 31 I AD3 I 12 29 I I AD3 I 13 28 I I AD1 I 15 26 I I AD1 I 15 26 I I AD1 I 17 24 I I NMI I 18 23 I I CLK I 19 22 I I	AD14 I 2 39 I AD15 AD13 I 3 38 I A16/S3 AD12 I 4 37 I A16/S3 AD14 I 5 36 I A16/S3 AD11 I 5 36 I A18/S5 AD10 I 6 35 I A18/S5 AD19 I 7 34 I BHE/S7 AD8 I 10 33 I MN/MX AD7 I 9 32 I RQ/GT0 AD5 I 12 29 I ICCK AD3 I 12 29 I ICCK AD3 I 12 28 I S2 AD2 I 14 27 I S1 AD1 I 15 26 I S0 AD1 I 17 24 I QS0 NMI I 18 23 I <td< th=""><th>AD14 I 2 39 AD15 AD13 I 3 38 I A16/S3 AD12 I 4 37 I A17/S4 AD11 I 5 36 I A18/S5 AD10 I 6 35 I A19/S6 AD19 I 7 34 I BHE/S7 AD8 I 8 33 I MN/MX AD7 I 9 32 I RQ/GT0 AD5 I 11 S0 30 I RQ/GT1 AD4 I 12 29 I LOCK AD3 I 13 28 S2 S1 AD4 I 15 26 S0 S0 AD1 I 15 26 S0 S0 AD1 I 17 24 QS1 QS1 NMI I 18 23 TEST READY</th></td<>	AD14 I 2 39 AD15 AD13 I 3 38 I A16/S3 AD12 I 4 37 I A17/S4 AD11 I 5 36 I A18/S5 AD10 I 6 35 I A19/S6 AD19 I 7 34 I BHE/S7 AD8 I 8 33 I MN/MX AD7 I 9 32 I RQ/GT0 AD5 I 11 S0 30 I RQ/GT1 AD4 I 12 29 I LOCK AD3 I 13 28 S2 S1 AD4 I 15 26 S0 S0 AD1 I 15 26 S0 S0 AD1 I 17 24 QS1 QS1 NMI I 18 23 TEST READY

BHE / S₇ Pin 34 (Output)

- BHE stands for Bus High Enable.
- BHE signal is used to indicate the transfer of data over higher order data bus $(D_8 - D_{15})$.
- 8-bit I/O devices use this signal.
 - It is multiplexed with status pin S_7 .

Vss (GND)	L 1		40	Vcc (5P)	
AD14	C 2		39	AD15	
AD13	C 3		38	A16/S3	
AD12	L 4		37	A17/S4	
AD11	D 5		36	A18/S5	
AD10	C 6		35	A19/S6	
AD9	Π 7		34	BHE/S7	
AD8	8		33	MIN/MX	
AD7	D 9		32	RD	
AD6	[10	86	31	RQ/GT0	HOLD
AD5	[11	8086	30	RQ/GT1	HLDA
AD4	[12	ω	29		WR
AD3	□ 13		28	3 <u>52</u>	M/IO
AD2	[14		27	<u> </u>	DT/R
AD1	C 15		26	SO	DEN
ADO	1 6		25		ALE
NML	[17		24	QS1	INTA
INTR	[18		23	TEST	
CLK	[19		22	READY	
Vss (GND)	□ 20		21	RESET	

RD (Read) Pin 32 (Output)

- It is a read signal used for read operation.
- It is an output signal.
- It is an active low signal.

١	/ss (GND)	C	1		40	ב	Vcc (5P)	
	AD14	C	2		39]	AD15	
	AD13	E	3		38]	A16/S3	
	AD12		4		37		A17/S4	
	AD11	C	5		36		A18/S5	
	AD10	C	6		35]	A19/S6	
	AD9	C	7		34]	BHE/S7	
	AD8	C	8		33	ב	MN/MX	
	AD7	C	9		32	כ	RD	
	AD6	C	10	86	31	כ	RQ/GTO	HOLD
	AD5	C	11	8086	30]	RQ/GT1	HLDA
	AD4	C	12	Ű	29		LOCK	WR
	AD3	С	13		28]	<u>S2</u>	M/ IO
	AD2	C	14		27		<u>S1</u>	DT/R
	AD1	E	15		26]	SO	DEN
	AD0	С	16		25]	QS0	ALE
	NMI	C	17		24		QS1	INTA
	INTR	С	18		23		TEST	
	CLK	C	19		22	3	READY	
1	/ss (GND)	C	20		21		RESET	

READY Pin 22 (Input)

- This is an acknowledgement signal from slower I/O devices or memory.
- It is an active high signal.
- When high, it indicates that the device is ready to transfer data.
- When low, then microprocessor is in wait state.

٧	'ss (GND)	C	1	\sim	40	þ	Vcc (5P)	
	AD14	C	2		39		AD15	
	AD13	E	3		38	Þ	A16/S3	
	AD12	C	4		37	þ	A17/S4	
	AD11	C	5		36		A18/S5	
	AD10	E	6		35	þ	A19/S6	
	AD9	C	7		34		BHE/S7	
	AD8	C	8		33	Þ	MN/MX	
	AD7	E	9		32	þ	RD	
	AD6	C	10	86	31	þ	RQ/GT0	HOLD
	AD5	C	11	8086	30	Þ	RQ/GT1	HLDA
	AD4	E	12		29	þ	LOCK	WR
	AD3	C	13		28		<u>52</u>	M/IO
	AD2	C	14		27	þ	<u>S1</u>	DT/R
	AD1	E	15		26	þ	SO	DEN
	AD0	C	16		25		QS0	ALE
	NMI	Ć	17		24	Þ	QS1	INTA
	INTR	E	18		23		TEST	
	CLK	C	19		22		READY	
V	ss (GND)	C	20		21		RESET	

RESET Pin 21 (Input)

- It is a system reset.
- It is an active high signal.
- When high, microprocessor enters into reset state and terminates the current activity.
 - It must be active for at least four clock cycles to reset the microprocessor.

٧	/ss (GND)	C	1	$\overline{\mathbf{v}}$	40		Vcc (5P)	
	AD14	C	2		39		AD15	
	AD13	E	3		38	Þ	A16/S3	
	AD12	C	4		37		A17/S4	
	AD11	C	5		36		A18/S5	
	AD10	C	6		35	þ	A19/S6	
	AD9	C	7		34		BHE/S7	
	AD8	C	8		33	۵	MN/MX	
	AD7	C	9		32	þ	RD	
	AD6	C	10	86	31		RQ/GT0	HOLD
	AD5	C	11	8086	30		RQ/GT1	HLDA
	AD4	E	12	~~	29		LOCK	WR
	AD3	C	13		28		<u>52</u>	M/ IO
	AD2	C	14		27		<u>S1</u>	DT/R
	AD1	C	15		26		SO	DEN
	AD0	C	16		25		QS0	ALE
	NML	C	17		24		QS1	INTA
	INTR	C	18		23		TEST	
	CLK	C	19		22	Þ	READY	
V	/ss (GND)	C	20		21		RESET	
								100 C

INTR Pin 18 (Input)

- It is an interrupt request signal.
- It is active high.
- It is level triggered.

'ss (GND)	C	1		40	þ	Vcc (5P)	
AD14	C	2		39		AD15	
AD13	E	3		38		A16/S3	
AD12	C	4		37		A17/S4	
AD11	C	5		36		A18/S5	
AD10	C	6		35		A19/S6	
AD9	C	7		34		BHE/S7	
AD8	C	8		33		MN/MX	
AD7	E	9		32		RD	
AD6	C	10	86	31		RQ/GT0	HOLD
AD5	C	11	ö	30		RQ/GT1	HLDA
AD4	C	12	Ű	29		LOCK	WR
AD3	С	13		28		S2	M/ IO
AD2	C	14		27		<u>S1</u>	DT/R
AD1	E	15		26		SO	DEN
ADO	C	16		25		QS0	ALE
NML	C	17		24		QS1	INTA
INTR		18		23		TEST	
CLK		19		22		READY	
'ss (GND)	C	20		21		RESET	
	AD13 AD12 AD11 AD10 AD9 AD8 AD7 AD6 AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0 NMI INTR	AD14 AD13 AD12 AD11 AD10 AD9 AD8 AD7 AD6 AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD2 AD1 AD0 NM1 NM1	AD14 AD13 AD13 AD12 4 AD11 5 AD10 5 AD10 AD11 5 AD10 AD10 AD11 5 AD10 AD10 AD10 AD10 AD10 AD10 AD10 AD10 AD10 AD3 AD10 AD3 AD10 AD10 AD10 AD10 AD10 AD11 AD10 AD11 AD11	AD14 2 AD13 4 AD12 4 AD12 4 AD11 5 AD10 6 AD9 7 AD8 8 AD7 9 AD6 10 AD5 11 AD4 12 AD3 13 AD2 14 AD1 15 AD0 16 NM1 17 INTR 18 CLK 19	AD14 2 39 AD13 3 38 AD12 4 37 AD11 5 36 AD11 5 36 AD10 6 35 AD9 7 34 AD8 8 33 AD7 9 32 AD6 10 99 32 AD6 11 80 30 AD4 12 29 AD3 13 28 AD2 14 27 AD1 15 26 AD0 16 25 NMI 17 24 INTR 18 23 CLK 19 22	AD14 2 39 AD13 3 38 AD12 4 37 AD11 5 36 AD11 5 36 AD10 6 35 AD9 7 34 AD8 8 33 AD7 9 32 AD6 10 99 AD5 11 30 AD4 12 29 AD3 13 28 AD2 14 27 AD1 15 26 AD0 16 25 NMI 17 24 INTR 18 23 19 22 1	AD14 2 39 AD15 AD13 3 38 AD15 AD12 4 37 A16/S3 AD11 5 36 A17/S4 AD11 5 36 A18/S5 AD10 6 35 A19/S6 AD9 7 34 BHE/S7 AD8 8 33 MN/MX AD7 9 32 RD AD6 10 8 33 MN/MX AD7 9 32 RQ/GT0 AD6 10 8 33 RQ/GT1 AD4 12 29 LOCK AD3 13 28 S2 AD2 14 27 S1 AD1 15 26 S0 AD0 16 25 QS0 NMI 17 24 QS1 INTR 18 23 TEST CHK 19 22 READY

NMI Pin 17 (Input)

It is a non-maskable interrupt signal.
It is an active high.
It is an edge triggered interrupt.

L 1	\sim	40		Vcc (5P)	
C 2		39		AD15	
C 3		38		A16/S3	
C 4		37		A17/S4	
C 5		36		A18/S5	
D 6		35		A19/S6	
D 7		34		BHE/S7	
8		33		MN/MX	
D 9		32		RD	
□ 10	86	31		RQ/GT0	HOLD
[11	ö	30		RQ/GT1	HLDA
[12		29		LOCK	WR
□ 13		28		<u>52</u>	M/IO
1 4		27		<u>S1</u>	DT/R
[15		26		SO	DEN
16		25		QS0	ALE
[17		24		QS1	INTA
1 8		23		TEST	
□ 19		22		READY	
20		21		RESET	
	 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 	 2 3 4 5 6 7 8 9 10 9808 11 12 13 14 15 16 17 18 19 	2 39 3 38 4 37 5 36 7 34 8 33 9 32 10 9808 31 11 30 12 29 13 28 14 27 15 26 16 25 17 24 18 23 19 22	2 39 3 38 4 37 5 36 7 34 8 33 9 32 10 80 90 31 11 30 12 29 13 28 14 27 15 26 16 25 17 24 18 23 19 22	2 39 AD15 3 38 A16/S3 4 37 A16/S3 5 36 A18/S5 6 35 A19/S6 7 34 BHE/S7 8 33 MN/MX 9 32 RD 10 9 31 RQ/GT0 11 28 S2 ICOCK 13 28 S2 S1 14 27 S1 S1 15 26 S0 S0 16 25 QS0 S1 17 24 QS1 TEST 18 22 READY



 It is used to test the status of math coprocessor 8087.

- The BUSY pin of 8087 is connected to this pin of 8086.
- If low, execution continues else microprocessor is in wait state.

V	/ss (GND)	E	1	\sim	40	þ	Vcc (5P)	
	AD14	C	2		39		AD15	
	AD13	C	3		38	þ	A16/S3	
	AD12	C	4		37	þ	A17/S4	
	AD11	C	5		36	þ	A18/S5	
	AD10	E	6		35	þ	A19/S6	
	AD9	C	7		34	þ	BHE/S7	
	AD8	C	8		33	þ	MN/MX	
	AD7	E	9		32	þ	RD	
	AD6	C	10	86	31	þ	RQ/GT0	HOLD
	AD5	C	11	8086	30	þ	RQ/GT1	HLDA
	AD4	E	12		29	þ	LOCK	WR
	AD3	C	13		28	þ	<u>52</u>	M/IO
	AD2	C	14		27	þ	<u>S1</u>	DT/R
	AD1	E	15		26	þ	SO	DEN
	AD0	C	16		25	þ	QS0	ALE
	NMI	C	17		24		QS1	INTA
	INTR	E	18		23		TEST	
	CLK	C	19		22	þ	READY	
V	/ss (GND)	C	20		21	þ	RESET	

CLK Pin 19 (Input)

 This clock input provides the basic timing for processor operation.

 It is symmetric square wave with 33% duty cycle.

 The range of frequency of different versions is 5 MHz, 8 MHz and 10 MHz.

		× .						
Vss	(GND)		1	$\overline{\mathbf{v}}$	40	þ	Vcc (5P)	
	AD14	C	2		39	þ	AD15	
	AD13	٥	3		38	þ	A16/S3	
	AD12		4		37	þ	A17/S4	
	AD11	C	5		36	þ	A18/S5	
	AD10	۵	6		35	þ	A19/S6	
	AD9		7		34	þ	BHE/S7	
	AD8	Ć	8		33	þ	MN/MX	
	AD7	٥	9		32	þ	RD	
	AD6		10	86	31	þ	RQ/GT0	HOLE
	AD5	۵	11	8086	30	þ	RQ/GT1	HLDA
	AD4		12		29	þ	LOCK	WR
	AD3		13		28	þ	<u>52</u>	M/IO
	AD2	٥	14		27	þ	<u>S1</u>	DT/R
	AD1	٥	15		26	þ	SO	DEN
	AD0		16		25	þ	QS0	ALE
	NMI	۵	17		24	þ	QS1	INTA
	INTR	Ę	18		23	þ	TEST	
	CLK	¢	19		22	þ	READY	
Vss	(GND)	ł	20		21	þ	RESET	

V_{CC} and V_{SS} Pin 40 and Pin 20 (Input)

- V_{CC} is power supply signal.
- +5V DC is supplied through this pin.
- V_{SS} is ground signal.

						1			
1	Vss (GND)	٢	1	\sim	40	þ	Vcc (5P)		
	AD14		2		39		AD15		
	AD13	E	3		38	þ	A16/S3		
	AD12	С	4		37		A17/S4		
	AD11	C	5		36	þ	A18/S5		
	AD10	C	6		35	þ	A19/S6		
	AD9	C	7		34		BHE/S7		
	AD8	٢	8		33	þ	MN/MX		
	AD7	٢	9		32	þ	RD		
	AD6	C	10	86	31	þ	RQ/GT0	H	OLD
	AD5	٢	11	8086	30	þ	RQ/GT1	НΙ	DA
	AD4	Ε	12		29	þ	LOCK	W	R
	AD3		13		28	Þ	S2	M/	10
	AD2		14		27	þ	S1	D	r/ <mark>R</mark>
	AD1	٢	15		26	þ	SO	DE	ΞN
	ADO		16		25		QS0	AL	E
	NML	٢	17		24	þ	QS1	ĪN	TA
	INTR	С	18		23	Þ	TEST		
	CLK	С	19		22		READY		
	Vss (GND)	С	20		21	Þ	RESET		
1									

MN/MX Pin 33 (Input)

- 8086 works in two modes:
 - Minimum Mode
 - Maximum Mode
- If MN/MX is high, it works in minimum mode.
- If MN/MX is low, it works in maximum mode.

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٧	/ss (GND)	C	1	$\overline{\mathbf{v}}$	40		Vcc (5P)	
	AD14	C	2		39	Þ	AD15	
	AD13	E	3		38	Þ	A16/S3	
	AD12	C	4		37		A17/S4	
	AD11	٦	5		36		A18/S5	
	AD10	C	6		35	þ	A19/S6	
	AD9		7		34	Þ	BHE/S7	
	AD8	C	8		33		MN/MX	
	AD7	E	9		32		RD	
	AD6	C	10	86	31		RQ/GT0	HOLD
	AD5	٦	11	8086	30		RQ/GT1	HLDA
	AD4	E	12	~~	29	þ	LOCK	WR
	AD3	С	13		28		<u>52</u>	M/ IO
	AD2	٦	14		27	Þ	<u>S1</u>	DT/R
	AD1	E	15		26	þ	SO	DEN
	AD0	C	16		25		QS0	ALE
	NMI	٦	17		24		QS1	INTA
	INTR	Γ	18		23	Þ	TEST	
	CLK		19		22		READY	
V	/ss (GND)	C	20		21	Þ	RESET	

MN/MX Pin 33 (Input)

- Pins 24 to 31 issue two different sets of signals.
- One set of signals is issued when CPU operates in minimum mode.
- Other set of signals is issued when CPU operates in maximum mode.

		Z					
Vss ((GND)		1	\sim	40	Vcc (5P)	
	AD14	۵	2		39	AD15	
1	AD13	۵	3		38	A16/S3	
	AD12	۵	4		37	A17/S4	
	4D11	۵	5		36	A18/S5	
1	AD10	٥	6		35	A19/S6	
	AD9	۵	7		34	BHE/S7	
	AD8	۵	8		33	MN/MX	
	AD7	C	9		32	RD	
	AD6		10	36	31	RQ/GT0	HOLD
	AD5	۵	11	8086	30	RQ/GT1	HLDA
	AD4	۵	12		29	LOCK	WR
	AD3	۵	13		28	<u>52</u>	M/ IO
	AD2	۵	14		27	<u>S1</u>	DT/R
	AD1	۵	15		26	SO	DEN
	AD0	۵	16		25	QS0	ALE
	NMI	۵	17		24	QS1	INTA
	INTR	С	18		23	TEST	
	CLK		19		22	READY	
Vss ((GND)		20		21	RESET	

Pin Description for Minimum Mode

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- This is an interrupt acknowledge signal.
- When microprocessor receives INTR signal, it acknowledges the interrupt by generating this signal.
- It is an active low signal.

٧	/ss (GND)	C	1	$\overline{\mathbf{v}}$	40	þ	Vcc (5P))		
	AD14	C	2		39	Þ	AD15			
	AD13	E	3		38	Þ	A16/S3			
	AD12	C	4		37	Þ	A17/S4			
	AD11	C	5		36		A18/S5			
	AD10	C	6		35	þ	A19/S6			
	AD9	C	7		34		BHE/S7			
	AD8	C	8		33	٥	MN/MX			
	AD7	C	9		32	þ	RD			
	AD6	C	10	86	31		RQ/GT0	1	HOLD	
	AD5	C	11	8086	30	Þ	RQ/GT1		HLDA	
	AD4	E	12	~~	29	þ	LOCK		WR	
	AD3	C	13		28		<u>52</u>		M/IO	
	AD2	C	14		27	þ	<u>S1</u>		DT/R	
	AD1	C	15		26	þ	SO		DEN	
	ADO	C	16		25		QS0	_	ALE	
	NML	C	17		24	þ	QS1		INTA	
	INTR	C	18		23	þ	TEST	_	<u> </u>	
	CLK	С	19		22		READY			
V	/ss (GND)	C	20		21	Þ	RESET			
	· · · · · · · · · · · · · · · · · · ·									



- This is an Address Latch Enable signal.
- It indicates that valid address is available on bus AD₀ – AD₁₅.
- It is an active high signal and remains high during T₁ state.
- It is connected to enable pin of latch 8282.

V	/ss (GND)		1	$\overline{\mathbf{v}}$	40	þ	Vcc (5P)		
	AD14	C	2		39		AD15			
	AD13	۵	3		38	þ	A16/S3			
	AD12		4		37		A17/S4			
	AD11	۵	5		36		A18/S5			
	AD10	۵	6		35		A19/S6			
	AD9		7		34		BHE/S7			
	AD8	Ć	8		33	þ	MN/MX			
	AD7	٥	9		32		RD			
	AD6		10	36	31		RQ/GTC	7	HOLD)
	AD5	۵	11	8086	30	۵	RQ/GT1		HLDA	
	AD4		12		29		LOCK		WR	
	AD3		13		28		<u>52</u>		M/IO	
	AD2	C	14		27		<u>S1</u>		DT/R	
	AD1	٥	15		26		SO		DEN	
	ADO		16		25		QS0		ALE	
	NML	۵	17		24		QS1		INTA	
	INTR	Γ	18		23		TEST			
	CLK		19		22		READY			
V	/ss (GND)	۵	20		21		RESET			



- This is a Data Enable signal.
- This signal is used to enable the transceiver 8286.
- Transceiver is used to separate the data from the address/data bus.
- It is an active low signal.

٧	/ss (GND)		1	\sim	40	þ	Vcc (5P))	
	AD14	C	2		39	Þ	AD15		
	AD13	E	3		38	þ	A16/S3		
	AD12	C	4		37	þ	A17/S4		
	AD11	٦	5		36	þ	A18/S5		
	AD10	C	6		35	þ	A19/S6		
	AD9	C	7		34		BHE/S7		
	AD8	C	8		33	þ	MN/MX		
	AD7	C	9		32	þ	RD		
	AD6	С	10	36	31		RQ/GT0	i	HOLD
	AD5	٦	11	8086	30	þ	RQ/GT1		HLDA
	AD4	C	12		29	þ	LOCK		WR
	AD3		13		28		<u>52</u>		M/IO
	AD2	C	14		27	þ	<u>S1</u>		DT/R
	AD1	E	15		26	þ	SO		DEN
	ADO	C	16		25		QS0		ALE
	NML	٢	17		24	þ	QS1		INTA
	INTR	Γ	18		23	þ	TEST		
	CLK		19		22		READY		
V	/ss (GND)	C	20		21	þ	RESET		

DT / R Pin 27 (Output)

- This is a Data Transmit/Receive signal.
- It decides the direction of data flow through the transceiver.
- When it is high, data is transmitted out.
- When it is low, data is received in.

V	ss (GND)		1	V	40	6	Vcc (5P))	
	AD14	C	2		39		AD15		
	AD13	E	3		38		A16/S3		
	AD12	E	4		37		A17/S4		
	AD11	C	5		36		A18/S5		
	AD10	C	6		35		A19/S6		
	AD9	C	7		34		BHE/S7		
	AD8	C	8		33		MN/MX		
	AD7	E	9		32		RD		
	AD6	C	10	86	31		RQ/GT0	i	HOLD
	AD5	C	11	8086	30		RQ/GT1		HLDA
	AD4	C	12	Ű	29		LOCK		WR
	AD3	C	13		28		<u>52</u>		M/IO
	AD2	C	14		27		<u>S1</u>		DT/R
	AD1	E	15		26		SO		DEN
	AD0	C	16		25		QS0		ALE
	NMI	C	17		24		QS1		INTA
	INTR	C	18		23		TEST		
	CLK	C	19		22		READY		
V	'ss (GND)		20		21		RESET		

M/IO Pin 28 (Output)

- This signal is issued by the microprocessor to distinguish memory access from I/O access.
- When it is high, memory is accessed.
- When it is low, I/O devices are accessed.

		Ζ.							
١	/ss (GND)		1	$\overline{\mathbf{v}}$	40	Þ	Vcc (5P)		
	AD14	۵	2		39		AD15		
	AD13	E	3		38	Þ	A16/S3		
	AD12		4		37	Þ	A17/S4		
	AD11	٦	5		36	Þ	A18/S5		
	AD10	E	6		35	þ	A19/S6		
	AD9		7		34		BHE/S7		
	AD8	C	8		33	þ	MN/MX		
	AD7	E	9		32	þ	RD		
	AD6		10	86	31		RQ/GT0	HOLD	
	AD5	٢	11	8086	30	þ	RQ/GT1	HLDA	
	AD4	E	12	w	29	þ	LOCK	WR	٦
	AD3		13		28		<u>52</u>	M/IO	
	AD2	C	14		27	þ	S1	DT/R	
	AD1	E	15		26	þ	SO	DEN	
	ADO		16		25		QS0	ALE	
	NML	٢	17		24	Þ	QS1	INTA	
	INTR	Γ	18		23	þ	TEST		
	CLK		19		22	þ	READY		
١	/ss (GND)	٦	20		21	þ	RESET		



- It is a Write signal.
- It is used to write data in memory or output device depending on the status of M/IO signal.
- It is an active low signal.

Vss (GND) [1	\sim	40	þ	Vcc (5P)			
AD1	4 C	2		39		AD15			
AD1	3 🗖	3		38	Þ	A16/S3			
AD1	2	4		37	Þ	A17/S4			
AD1	1 🗖	5		36		A18/S5			
AD1	ם כ	6		35	þ	A19/S6			
AD	9 🗖	7		34		BHE/S7			
AD	ВС	8		33	٥	MN/MX			
AD	7 🗖	9		32	þ	RD			
AD	6 C	10	86	31		RQ/GT0		HOLD	
AD	5 C	11	8086	30	Þ	RQ/GT1	-	HLDA	1
AD	4 C	12	~	29	þ	LOCK		WR	
AD:	3 C	13		28		<u>52</u>		M/IO	
AD:	2	14		27	Þ	<u>S1</u>		DT/R	
AD	1 E	15		26	þ	SO		DEN	
AD	D 🗆	16		25		QS0		ALE	
NM		17		24	þ	QS1		INTA	
INTE	2 2	18		23	þ	TEST			
CLł		19		22		READY			
Vss (GND) [20		21	þ	RESET			

HLDA Pin 30 (Output)

- It is a Hold Acknowledge signal.
- It is issued after receiving the HOLD signal.
- It is an active high signal.

٧	/ss (GND)	C	1	$\overline{\mathbf{v}}$	40	þ	Vcc (5P)			
	AD14	٦	2		39		AD15			
	AD13	E	3		38		A16/S3			
	AD12	C	4		37		A17/S4			
	AD11	۵	5		36		A18/S5			
	AD10	E	6		35		A19/S6			
	AD9	C	7		34		BHE/S7			
	AD8	C	8		33		MN/MX			
	AD7	E	9		32		RD			
	AD6	C	10	86	31		RQ/GT0	_	HOLD	h
	AD5	C	11	8086	30		RQ/GT1		HLDA	1
	AD4	E	12	ω.	29		LOCK		WR	7
	AD3	C	13		28		<u>52</u>		M/IO	
	AD2	C	14		27		S1		DT/R	
	AD1	E	15		26		SO		DEN	
	AD0	E	16		25		QSO		ALE	
	NMI	C	17		24		QS1		INTA	
	INTR	E	18		23		TEST			
	CLK	C	19		22		READY			
V	/ss (GND)	C	20		21		RESET			

HOLD Pin 31 (Input)

- When DMA controller needs to use address/data bus, it sends a request to the CPU through this pin.
- It is an active high signal.
- When microprocessor receives HOLD signal, it issues HLDA signal to the DMA controller.

		× .						
٧	/ss (GND)	C	1	\sim	40	þ	Vcc (5P)	
	AD14	۵	2		39		AD15	
	AD13	E	3		38	Þ	A16/S3	
	AD12		4		37	þ	A17/S4	
	AD11	۵	5		36	Þ	A18/S5	
	AD10	E	6		35	þ	A19/S6	
	AD9	E	7		34		BHE/S7	
	AD8	۵	8		33	þ	MN/MX	
	AD7	C	9		32	þ	RD _	
	AD6	С	10	36	31		RQ/GTC	HOLD
	AD5	۵	11	8086	30	þ	RQ/GT1	HLDA
	AD4	C	12		29	þ	LOCK	WR
	AD3	C	13		28		<u>52</u>	M/IO
	AD2	۵	14		27	þ	<u>S1</u>	DT/R
	AD1	E	15		26	þ	SO	DEN
	AD0	С	16		25		QS0	ALE
	NMI	۵	17		24	þ	QS1	INTA
	INTR	C	18		23	þ	TEST	
	CLK		19		22		READY	
V	/ss (GND)	С	20		21	þ	RESET	

Pin Description for Maximum Mode

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QS₁ and QS₀ Pin 24 and 25 (Output)

These pins provide the status of instruction queue.

QS ₁	QS ₀	Status
0	0	No operation
0	1	1 st byte of opcode from queue
1	0	Empty queue
1	1	Subsequent byte from queue

		×						
V	/ss (GND)		1	$\overline{\mathbf{v}}$	40	þ	Vcc (5P)	
	AD14		2		39	þ	AD15	
	AD13	٥	3		38	Þ	A16/S3	
	AD12		4		37		A17/S4	
	AD11		5		36		A18/S5	
	AD10		6		35	þ	A19/S6	
	AD9		7		34		BHE/S7	
	AD8		8		33	۵	MN/MX	
	AD7	۵	9		32	þ	RD	
	AD6		10	86	31		RQ/GT0	HOLD
	AD5		11	8086	30		RQ/GT1	HLDA
	AD4		12	~~	29		LOCK	WR
	AD3		13		28		<u>52</u>	M/ IO
	AD2		14		27		S1	DT/R
	AD1		15		26		SO	DEN
	AD0		16		25	۵	QS0	ALE
	NMI		17		24		QS1	INTA
	INTR	۵	18		23	þ	TEST	
	CLK		19		22		READY	
V	/ss (GND)		20		21		RESET	

S₀, **S**₁, **S**₂ Pin 26, 27, 28 (Output)

- These status signals indicate the operation being done by the microprocessor.
- This information is required by the Bus Controller 8288.
- Bus controller 8288 generates all memory and I/O control signals.

ſ	/ss (GND)	E	1	V	40	þ	Vcc (5l	P)	
	AD14	C	2		39		AD15		
	AD13	C	3		38	þ	A16/S3	3	
	AD12	C	4		37	þ	A17/S4	1	
	AD11	۵	5		36	þ	A18/S5	5	
	AD10	E	6		35	þ	A19/S6	6	
	AD9	E	7		34		BHE/S	7	
	AD8	C	8		33	þ	MN/M2	ζ	
	AD7	E	9		32	þ	RD		
	AD6	C	10	86	31		RQ/GT	0	HOLE
	AD5	C	11	8086	30	þ	RQ/GT	1	HLDA
	AD4		12		29	Þ	LOCK		WR
	AD3	C	13		28		<u>52</u>		M/ĪŌ
	AD2	C	14		27		<u>S1</u>		DT/R
	AD1	E	15		26		SO		DEN
	ADO	C	16		25	ם	QS0		ALE
	NMI	C	17		24	þ	QS1		INTA
	INTR	Е	18		23	þ	TEST		
	CLK	C	19		22	þ	READ	ſ	
l	/ss (GND)	C	20		21	þ	RESET	Г	

S₀, **S**₁, **S**₂ Pin 26, 27, 28 (Output)

S ₁	S ₀	Status
0	0	Interrupt Acknowledge
0	1	I/O Read
1	0	I/O Write
1	1	Halt
0	0	Opcode Fetch
0	1	Memory Read
1	0	Memory Write
1	1	Passive
	0 1 1 0	0 0 0 1 1 0 1 1 0 0 0 1

Vss (GND)	1	Y	40	ב	Vcc (5F))	
AD14 🗖	2		39		AD15		
AD13	3		38	٦	A16/S3		
AD12	4		37]	A17/S4		
AD11	5		36		A18/S5		
AD10	6		35]	A19/S6		
AD9 🗖	7		34]	BHE/S7	7	
AD8 🗖	8		33		MN/MX		
AD7 🕻	9		32]	RD		
AD6 🛽	10	86	31]	RQ/GT	ō	HOLD
AD5 🕻	11	8086	30]	RQ/GT	1	HLDA
AD4 🗖	12	~	29	ב	LOCK		WR
AD3 🛽	13		28	ב	<u>52</u>		M/IO
AD2	14		27	ב	<u>S1</u>		DT/R
AD1 🛽	15		26	כ	SO		DEN
ADO 🗖	16		25	נ	QS0		ALE
NMI 🕻	17		24		QS1		INTA
INTR	18		23		TEST		
CLK 🗖	19		22		READY	r	
vss (GND)	20		21		RESET		



- This signal indicates that other processors should not ask CPU to relinquish the system bus.
- When it goes low, all interrupts are masked and HOLD request is not granted.
- This pin is activated by using LOCK prefix on any instruction.

٧	ss (GND)	C	1	\sim	40	þ	Vcc (5P)	
	AD14	C	2		39	Þ	AD15	
	AD13	C	3		38	þ	A16/S3	
	AD12	C	4		37	þ	A17/S4	
	AD11	C	5		36		A18/S5	
	AD10	E	6		35	þ	A19/S6	
	AD9	C	7		34		BHE/S7	
	AD8	C	8		33	þ	MN/MX	
	AD7	E	9		32	þ	RD	
	AD6	E	10	86	31		RQ/GT0	HOLD
	AD5	C	11	8086	30	٥	RQ/GT1	HLDA
	AD4	E	12		29		LOCK	WR
	AD3	C	13		28	ם	<u>S2</u>	M/IO
	AD2	C	14		27	þ	<u>S1</u>	DT/R
	AD1	E	15		26	þ	SO	DEN
	ADO	E	16		25		QS0	ALE
	NML	C	17		24	Þ	QS1	INTA
	INTR	C	18		23	þ	TEST	
	CLK	C	19		22		READY	
V	'ss (GND)	C	20		21	þ	RESET	

RQ/GT₁ and RQ/GT₀ Pin 30 and 31 (Bi-directional)

- These are Request/Grant pins.
- Other processors request the CPU through these lines to release the system bus.
- After receiving the request, CPU sends acknowledge signal on the same lines.
- $\overline{RQ}/\overline{GT}_0$ has higher priority than $\overline{RQ}/\overline{GT}_1$.

٧	/ss (GND)		1	$\overline{\mathbf{v}}$	40		Vcc (5P)	
	AD14	۵	2		39	þ	AD15	
	AD13	E	3		38	þ	A16/S3	
	AD12		4		37		A17/S4	
	AD11		5		36		A18/S5	
	AD10	D	6		35	Þ	A19/S6	
	AD9		7		34	Þ	BHE/S7	
	AD8	۵	8		33		MN/MX	
	AD7	E	9		32	Þ	RD	
	AD6		10	8086	31		RQ/GT0	HOLD
	AD5		11	Ö	30		RQ/GT1	HLDA
	AD4	E	12	Ĩ	29	ם	LOCK	WR
	AD3		13		28	Þ	S2	M/IO
	AD2		14		27		<u>S1</u>	DT/R
	AD1	E	15		26	Þ	SO	DEN
	AD0		16		25	Þ	QS0	ALE
	NMI	۵	17		24		QS1	INTA
	INTR	C	18		23	þ	TEST	
	CLK		19		22		READY	
V	/ss (GND)		20		21		RESET	

Thank You [♥]♥ Have a Nice Day

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